WHAT IS CLAIMED IS:

1. A differential comparator having positive and negative inputs and positive and negative outputs, comprising:

a current source for driving current from a supply to a common node;

a differential pair of transistors having one side of the source/drain paths thereof tied together and to said common node and the other side of the source/drain paths thereof for each of the transistors in said differential pair interfaced to the positive and negative outputs, respectively for applying drive thereto;

a first resistor load disposed between said positive output and a supply reference opposite in polarity to the supply;

a second resistor disposed between said negative output and said supply reference;

the gate of the one of the transistors in said pair associated with said positive output connected to the negative input, and the gate of the other of the transistors in said pair connected to the positive input;

the current through said current source defining the common mode bias; and

a bias circuit for controlling the voltage on the first and second outputs at the first and second resistors to be at a common mode voltage that is controlled by an external bias voltage when the positive and negative inputs are at substantially the same voltage.

2. The differential comparator of Claim 1, wherein said bias circuit comprises a ratiometric bias circuit having associated therewith a bias resistor with a current driven there through, said ratiometric bias circuit controlling the current through said current source, such that it is a ratio of the current through said bias resistor.

3. The differential comparator of Claim 2, wherein said ratiometric circuit includes a bias current source for driving said bias resistor.

4. The differential comparator of Claim 3, wherein said bias current source comprises a voltage bias circuit for applying a voltage across said bias resistor substantially equal to the external bias voltage.

5. The differential comparator of Claim 4, wherein said current source comprises a drive transistor having the source/drain path thereof connected between the supply and said common node and the voltage on the gate thereof controlled by said ratiometric bias circuit.

6. The differential comparator of Claim 5, wherein said ratiometric bias circuit includes a bias transistor having the source/drain thereof connected between the supply and said bias resistor and the gate thereof driven by a driver to control the voltage across said bias resistor, wherein the current through said bias resistor and said bias transistor are the same and the gate of said drive transistor has a voltage on the gate thereof that is ratioed to the voltage on the gate of said bias transistor.

7. The differential comparator of Claim 6, wherein said driver comprises a unity gain voltage driver having a negative input for receiving the external bias voltage and an output for driving the gate of said bias transistor, the positive input thereof connected to said bias resistor.

8. The differential comparator circuit of Claim 2, wherein said ratiometric bias circuit includes:

a drive transistor having the source/drain path thereof connected between the supply and said common node;

a voltage driver that drives the gate of said drive transistor to apply the external bias voltage across said bias resistor such that the current there through is a direct function of the external bias voltage; and

a current reflection device for reflecting the current through said bias resistor and said drive transistor to the current through each of said first and second resistors, such that the current through said first and second resistors is a ratio of the current through said bias resistor.

9. The differential comparator of Claim 8, wherein said voltage driver comprises a unity gain voltage driver having a negative input for receiving the external bias voltage as an input and an output for driving the gate of said bias transistor, the positive input thereof connected to said bias resistor.

10. The differential comparator of Claim 9, wherein said current source comprises a drive transistor having the source/drain path thereof connected between the supply and said common node and the voltage on the gate thereof controlled by the output of said voltage driver, such that the voltage across said first and second resistors is substantially the external bias voltage.

11. A method for comparing positive and negative input signals on positive and negative inputs to provide positive and negative output signals on positive and negative outputs, comprising the steps of:

driving current from a supply to a common node with a current source;

disposing a differential pair of transistors with one side of the source/drain paths thereof tied together and to the common node and the other side of the source/drain paths thereof for each of the transistors in the differential pair interfaced to the positive and negative outputs, respectively for applying drive thereto;

disposing a first resistor load between the positive output and a supply reference opposite in polarity to the supply;

disposing a second resistor between the negative output and the supply reference;

the gate of the one of the transistors in the pair associated with the positive output connected to the negative input, and the gate of the other of the transistors in the pair connected to the positive input;

the current through the current source defining the common mode bias; and

controlling with a bias circuit the voltage on the first and second outputs at the first and second resistors to be at a common mode voltage that is controlled by an external bias voltage when the positive and negative inputs are at substantially the same voltage.

12. The method of Claim 11, wherein the bias circuit comprises a ratiometric bias circuit having associated therewith a bias resistor and including the step of driving a current there through, and the step of controlling with the ratiometric bias circuit the current through the current source, such that it is a ratio of the current through the bias resistor.

13. The method of Claim 12, wherein the ratiometric circuit includes a bias current source and including the step of driving the bias resistor with the bias current source.

14. The method of Claim 13, wherein the bias current source comprises a voltage bias circuit and including the step of applying a voltage across the bias resistor substantially equal to the external bias voltage.

15. The method of Claim 14, wherein the current source comprises a drive transistor having the source/drain path thereof connected between the supply and the common node and the voltage on the gate thereof controlled by the ratiometric bias circuit.

16. The method of Claim 15, wherein the ratiometric bias circuit includes a bias transistor having the source/drain thereof connected between the supply and the bias resistor and the gate thereof driven by a driver and including the step of controlling the voltage across the bias resistor with the driver, wherein the current through the bias resistor and the bias transistor are the same and the gate of the drive transistor has a voltage on the gate thereof that is ratioed to the voltage on the gate of the bias transistor.

17. The method of Claim 16, wherein the driver comprises a unity gain voltage driver having a negative input for receiving the external bias voltage and an output for driving the gate of the bias transistor, the positive input thereof connected to the bias resistor.

18. The method circuit of Claim 12, wherein the ratiometric bias circuit includes:

a drive transistor having the source/drain path thereof connected between the supply and the common node;

driving the gate of the drive transistor with a voltage driver to apply the external bias voltage across the bias resistor such that the current there through is a direct function of the external bias voltage; and

reflecting the current through the bias resistor and the drive transistor with a current reflection device to the current through each of the first and second resistors, such that the current through the first and second resistors is a ratio of the current through the bias resistor.

19. The method of Claim 18, wherein the voltage driver comprises a unity gain voltage driver having a negative input for receiving the external bias voltage as an input and an output for driving the gate of the bias transistor, the positive input thereof connected to the bias resistor.

20. The method of Claim 19, wherein the current source comprises a drive transistor having the source/drain path thereof connected between the supply and the common node and the voltage on the gate thereof controlled by the output of the voltage driver, such that the voltage across the first and second resistors is substantially the external bias voltage.